AMENDMENTS TO THE CLAIMS

What I claim as my invention is:

1. (Original) A fractional-N frequency synthesizer for generating the high frequency signal at frequency that may be a non-integer multiple of the frequency of the reference signal, having a voltage controlled oscillator (3) the output of which is fed to a first order Delta-Sigma frequency discriminator (4) having a dual modulus frequency divider (1) and a D flip-flop (2), where a bit stream related to the frequency and phase of said voltage controlled oscillator is generated by using said reference signal and is then processed to generate a feedback error signal by using the information provided by comparing said bit stream with a bit stream generated by an accumulator digitally performing the first order Delta-Sigma modulation to the desired fractional number for the controlling of said voltage controlled oscillator after the said feedback error signal is properly filtered, amplified and converted, which will maximally suppress the fractional spurs due to the frequency quantization of said Delta-Sigma frequency discriminator.

2. (Original) A frequency synthesizer according to claim 1 wherein said fractional number and said reference frequency is chosen with the help of design principle that non-reducible denominator of said fractional number has a close relation with the phase error performance of the synthesizer.

3. (Currently amended) A frequency synthesizer according to claim 1 ~~or claim 2~~ wherein ~~the said information provided by comparing said bit streams is used in such way that said feedback error signal represents the change of the phase of said voltage controlled oscillator relating to a standard signal established by said reference signal and said accumulator with an allowable shift on detection time~~ a feedback error signal representing the frequency error of said voltage controlled oscillator is generated when the comparing bits is different by using the information provided by the present sampling phase of the accumulator (8) on the lower limit of the phase difference generated by the said frequency error, and the same value as that of the said feedback error signal will be used as the rotating angle to restart said accumulate (8) after the error signal generation so that the detected phase

error generated by the frequency error of said voltage controlled oscillator will not interfere, and the undetected phase error will be kept, for the error detection in the following detection cycles.

4. (Original) A frequency synthesizer according to claim 3 wherein said feedback error signal is set to 0 if the two comparing bits from said bit streams equal in value, and is set to the sampling phase of said accumulator if the two comparing bits from said bit streams not equal in value while said accumulator will be restarted by sending 2 times its present output bit minus 1 to its feedback input for the operation of next reference cycle.

5. (Currently amended) A frequency synthesizer according to ~~claim 3 or~~ claim 4 wherein said feedback error signal contains a small perturbation signal applied according to the change of the output bit of said Delta-Sigma frequency discriminator on the cycle that the sampling phase of said accumulator is 0 with fixed amplitude but proper sign so that the phase error of said voltage controlled oscillator is confined to a small range.

6. (Currently amended) A frequency synthesizer according to claim 5 wherein the sum of all the perturbation signal applied after the last time to send the sampling phase of said accumulator as the feedback signal and subsequently restart said accumulator will be subtracted from the sampling phase of said accumulator if its sampling phase will be sent as the feedback error signal for this reference cycle, so that the loop could seamlessly switch back to the operation mode with no perturbations ~~as described by claim 3~~.

7. (Currently amended) A frequency synthesizer according to ~~all of above claims~~ claim 1 wherein said feedback error signal is filtered by a digital loop filter (10) for getting the required loop transfer function and subsequently converted by a digital to analog converter (6) to an analogue control voltage that will be fed back via an analogue low pass filter (7) to said voltage controlled oscillator for controlling its frequency.

8. (Currently amended) A frequency synthesizer according to ~~all of above claims~~ claim 7 wherein said loop filter has an additional integrator that will form the

synthesizer using said Delta-Sigma frequency discriminator as a phase-locked-loop.

9. (Currently amended) A frequency synthesizer according to ~~all of above claims except claim 8~~ claim 7 wherein the synthesizer is formed to be a frequency-locked-loop in order to optimize its noise performance and transient response characteristics for a specific application.

10. (Original) A frequency synthesizer according to claim 7 wherein that its loop bandwidth and the loop formation as a phase-locked-loop or frequency-locked-loop could be dynamically changed during the operation with the help of digital implementation to get fast lock-in time at the start up and high performance in normal working stage.

11. (Currently amended) A frequency or phase modulator that is based on the frequency synthesizer according to ~~all of above claims~~ claim 1 wherein a modulation signal in the format of normalized frequency deviation is combined with said fractional number S and sent to said accumulator to perform the modulation.

12. (Original) A frequency or phase modulator according to claim 11 wherein said modulation signal in the format of frequency deviation is also combined with the output from said loop filter to perform two points wideband modulation.

13. (Original) A frequency or phase modulator according to claim 12 wherein that the gain of said voltage controlled oscillator is calibrated by using a low frequency scanning modulation applied to the modulation point to the accumulator and then check the output of the loop filter generated by the loop feedback.

14. (Original) A frequency or phase modulator according to claim 12 wherein that the gain of said voltage controlled oscillator is calibrated by locking the loop to several frequency points and checking the output of the loop filter generated by the loop feedback for these frequencies, while the calibration time could be reduced by switching the loop bandwidth or formation.

15. (Original) A frequency or phase modulator according to claim 12 that the change on the gain of said voltage controlled oscillator could be estimated and

compensated during the normal operation by estimating the magnitude of modulation component in the feedback error signal.

16. (Original) A frequency or phase modulator according to claim 12 that the change on the gain of said voltage controlled oscillator could be estimated and compensated during the normal operation by performing a high pass filtering to the modulation signal combined with the output from said loop filter and measuring the amplitude of the low frequency component provided by the loop feedback mechanism from said loop filter to cancellation the effect of said high pass filtering.

17. (Currently amended) A frequency synthesizer or modulator has the working principal according to ~~one of above claims~~ claim 1 wherein said dual modulus frequency divider used in said Delta-Sigma frequency discriminator has two division moduli that is separated by more than one.

18. (Currently amended) A frequency synthesizer or modulator has the working principal according to ~~one of above claims~~ claim 1 wherein said Delta-Sigma frequency discriminator has a reset circuit to remove the initial phase mismatch between said DMD output and said reference signal.